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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/564,626	02/23/2006	Sumio Ogawa	Q92356	2062

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EXAMINER	
LE, THONG QUOC	

ART UNIT	PAPER NUMBER
2827	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	04/27/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	10/564,626	OGAWA ET AL.	
	Examiner	Art Unit	
	Thong Q. Le	2827	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *13 January 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-6,8 and 11-15* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-6,8 and 11-15* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *01/13/1006, 02/23/2006*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. Pre-amendment filed on 01/13/2006 has been entered.

2. Claims 1-6, 8, 11-15 are presented for examination.

Information Disclosure Statement

3. This office acknowledges receipt of the following items from the Applicant:

Information Disclosure Statement (IDS) filed on 01/13/2006.

Information Disclosure Statement (IDS) filed on 02/23/2006.

4. Information disclosed and list on PTO 1449 was considered.

Specification

5. The lengthy specification has not been checked to the extent necessary to determine the presence of all possible minor errors. Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

Double Patenting

6. A rejection based on double patenting of the "same invention" type finds its support in the language of 35 U.S.C. 101 which states that "whoever invents or discovers any new and useful process ... may obtain a patent therefor ..." (Emphasis added). Thus, the term "same invention," in this context, means an invention drawn to identical subject matter. See *Miller v. Eagle Mfg. Co.*, 151 U.S. 186 (1894); *In re Ockert*, 245 F.2d 467, 114 USPQ 330 (CCPA 1957); and *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970).

A statutory type (35 U.S.C. 101) double patenting rejection can be overcome by canceling or amending the conflicting claims so they are no longer coextensive in

scope. The filing of a terminal disclaimer cannot overcome a double patenting rejection based upon 35 U.S.C. 101.

7. Claim 6 is objected to under 37 CFR 1.75 as being a substantial duplicate of claim 5. When two claims in an application are duplicates or else are so close in content that they both cover the same thing, despite a slight difference in wording, it is proper after allowing one claim to object to the other as being a substantial duplicate of the allowed claim. See MPEP § 706.03(k).

Regarding claims 5 and 6, claim 6 is repeated claim 5.

Claim Rejections - 35 USC § 102

8. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

9. Claims 1-6, 8, 11-15 are rejected under 35 U.S.C. 102(b) as being anticipated by Nagai (Pub. U.S. Patent No. 2001/0055233).

Regarding claim 1, Nagai discloses a semiconductor memory device which has a redundancy circuit (ABSTRACT, Figure 4) comprising:

a plurality of memory blocks (([0004]) ; and

a plurality of redundancy memory blocks ([0004]) provided for each of said plurality of memory blocks,

wherein each of said plurality of memory blocks includes a plurality of segments (Figure 2),

said plurality of segments are adjacent to one after another (Figure 2),

segments having defects among said plurality of segments are dispersively allocated to said plurality of redundancy memory blocks and replaced by said allocated redundancy memory blocks (Figures 1, 2, 10, 11, NCD for normal memory, SCD for spare memory, [0084-0085], [0087], [0097]).

Regarding claim 2, Nagai discloses each of the plurality of segments includes one or more adjacent memory cell rows or one or more adjacent memory column (Figures 2, 10,11).

Regarding claim 3, Nagai discloses wherein position of an address bit for selecting the plurality of memory blocks is different from a position of an address for selecting the plurality of redundancy blocks (Figure 3, [0095-0097]).

Regarding claim 4, Nagai discloses wherein address bits that defined the plurality of segments are lower address bits, and address bits for selecting the plurality of redundancy memory blocks include an address bit immediately above the lower address bits ([0009], [0020], Figure 14).

Regarding claims 5-6, Nagai discloses a semiconductor memory device (Figure 1) comprising:

a memory block having a plurality of segments (Figure 2) , each of said plurality of segments including a plurality of memory cells; and

a plurality of redundancy memory blocks (ABSTRACT, Figure 1, 16 spare word line) which are provided for said memory block

wherein each of said plurality of redundancy memory blocks has a redundancy segment which substitutes for any segment having a defect among said plurality of segments ([0004]),

said plurality of segments are allocated to said plurality of redundancy memory blocks (Figure1, 2), a number indicating said redundancy memory block allocated to said any segment is given by a remainder generated when an address indicating said any segment is divided by a number of said plurality of redundancy memory blocks ([0017-0021]), and

each of said plurality of segments is replaceable by said redundancy segment of said allocated redundancy memory block when having a defect ([0004]).

Regarding claim 8, Nagai discloses wherein a first segment and a second segment of said plurality of segments are adjacent to each other, and a first redundancy memory block allocated to said first segment and a second redundancy memory block allocated to said second segment are different redundancy memory blocks (Figures 1, 2 where NRD, SRD in different segment).

Regarding claims 11, 14, Nagai discloses wherein each of the plurality of segments is a group of memory cells connected to 2n, word lines or bit lines, the word lines are adjacent to one after another when a number of the word lines is a plural, and the bit lines are adjacent to one after another when a number of the bit lines is a plural ([0020]).

Regarding claim 12, Nagai discloses wherein a plurality of lower bits of an address inputted to a decode circuit for selecting any of said plurality of segments are inputted to a decode circuit for selecting said redundancy memory blocks (Figure 3).

Regarding claim 13, Nagai discloses wherein a first segment and a second segment of said plurality of segments are adjacent to each other, and a first redundancy memory block allocated to said first segment and a second redundancy memory block allocated to said second segment are different redundancy memory blocks (Figure 2, NCD for normal cell, SCD for redundancy cell).

Regarding claim 15, Nagai discloses wherein a plurality of lower bits of an address inputted to a decode circuit for selecting any of said plurality of segments are inputted to a decode circuit (Figure 3, 34, 31) for selecting said redundancy memory blocks (Figure 3).

10. Claims 1-6, 8, 11-15 are rejected under 35 U.S.C. 102(b) as being anticipated by Chung et al. (U.S. Patent No. 6,154,389).

Regarding claim 1, Chung et al. disclose a semiconductor memory device which has a redundancy circuit (ABSTRACT, Figure14) comprising:

a plurality of memory blocks (Figure1A) ; and

a plurality of redundancy memory blocks (Figure 1B) provided for each of said plurality of memory blocks,

wherein each of said plurality of memory blocks includes a plurality of segments (Figure 2),

said plurality of segments are adjacent to one after another (Figure 2),

segments having defects among said plurality of segments are dispersively allocated to said plurality of redundancy memory blocks and replaced by said allocated redundancy memory blocks (Column 2, lines 9-60).

Regarding claim 2, Chung et al. disclose each of the plurality of segments includes one or more adjacent memory cell rows or one or more adjacent memory column (Figures 2).

Regarding claim 3,Chung et al. disclose wherein position of an address bit for selecting the plurality of memory blocks is different from a position of an address for selecting the plurality of redundancy blocks (Figure 2).

Regarding claim 4, Chung et al. disclose wherein address bits that defined the plurality of segments are lower address bits, and address bits for selecting the plurality of redundancy memory blocks include an address bit immediately above the lower address bits (Figure 2).

Regarding claims 5-6, Chung et al. disclose a semiconductor memory device (Figure 1) comprising:

a memory block having a plurality of segments (Figure 1A) , each of said plurality of segments including a plurality of memory cells; and

a plurality of redundancy memory blocks (Figure 1B) which are provided for said memory block

wherein each of said plurality of redundancy memory blocks has a redundancy segment which substitutes for any segment having a defect among said plurality of segments (Column 2, lines 10-60),

said plurality of segments are allocated to said plurality of redundancy memory blocks (Figure 1B), a number indicating said redundancy memory block allocated to said any segment is given by a remainder generated when an address indicating said any segment is divided by a number of said plurality of redundancy memory blocks (Column 2, lines 10-46), and

each of said plurality of segments is replaceable by said redundancy segment of said allocated redundancy memory block when having a defect (Column3, lines 31-43]).

Regarding claim 8, Chung et al. disclose wherein a first segment and a second segment of said plurality of segments are adjacent to each other, and a first redundancy memory block allocated to said first segment and a second redundancy memory block allocated to said second segment are different redundancy memory blocks (Figures 1A, 1B).

Regarding claims 11, 14, Chung et al. disclose wherein each of the plurality of segments is a group of memory cells connected to 2n, word lines or bit lines, the word lines are adjacent to one after another when a number of the word lines is a plural, and the bit lines are adjacent to one after another when a number of the bit lines is a plural (Figure 2).

Regarding claims 12, 15, Chung et al. disclose wherein a plurality of lower bits of an address inputted to a decode circuit for selecting any of said plurality of segments

are inputted to a decode circuit (Figure 2, 120, 150) for selecting said redundancy memory blocks..

Regarding claim 13, Chung et al. disclose wherein a first segment and a second segment of said plurality of segments are adjacent to each other, and a first redundancy memory block allocated to said first segment and a second redundancy memory block allocated to said second segment are different redundancy memory blocks (Figure 2, 110, 140).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thong Q. Le whose telephone number is 571-272-1783. The examiner can normally be reached on 8:00am-5:00pm M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Zarabian Amir can be reached on 571-272-1852. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only.

For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Thong Q. Le
Primary Examiner
Art Unit 2827